Discontinuous-Current-Source Drivers for High-Frequency Power MOSFETs

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***Abstract*—This paper proposes a new current-source driver (CSD) with discontinuous inductor current. Compared to other CSDs proposed in the previous work, the most important advantage of the proposed CSD is the small inductance (typically, 20 nH at 1 MHz switching frequency). This translates into the footprint reduction of as much as 90% compared with the continuous CSDs. Other features of the proposed CSD includes: 1) fast switching speed and reduced switching loss; 2) discontinuous inductor current with low circulating loss; 3) gate energy recovery; and 4) wide range of duty cycle and switching frequency. The experimental results verified the functionality of the proposed CSD. At 12 V input, 1.3 V output, and 1 MHz switching frequency, the new CSD improves the efficiency from 80.7% using a conventional driver to 85.7% at 25 A output, and at 30 A output, from 77.9% to 84.4%.**

***Index Terms*—Buck converter, current-source driver (CSD), power MOSFET, resonant gate driver, voltage regulator (VR), voltage regulator module (VRM).**

I. Introduction

RESONANT gate driver technique was originally used to recover high gate-drive loss in high-frequency (typically, 5–10 MHz) resonant converters [1]–[3]. Self-oscillating resonant gate driver (soft gating driver) with a resonant network was used in radio frequency power amplifiers (>30 MHz) featuring sinusoidal waveforms [4]–[6].

Recently, resonant gate driver technique has been used in high current and low voltage application, such as voltage regulators (VRs). For a conventional voltage-source driver, all the gate-drive energy is dissipated through resistances in series with the gate capacitor and this drive loss is often called CV^2 loss. In VR applications, synchronous rectifier (SR) technique is widely used to reduce high conduction loss of freewheeling diodes. However, SR MOSFETs normally have high gate-drive loss due to the large total gate charge. At the same time, the gate-driver loss is proportional to the switching frequency. Therefore, the gate-driver loss becomes a penalty when the switching frequency is beyond 1 MHz, since the switching frequency of VRs has been moved into megahertz range. The excessive gate loss, not only decreases the overall efficiency but also makes the driver chips hotspots in the whole power supply system.

Different resonant driver topologies have been proposed to reduce the gate-drive loss [7]–[11]. A resonant gate driver with simple configuration was proposed in [12]. A nonisolated resonant gate driver was proposed for the interleaving boost converters in [13]. An isolated resonant gate-drive circuit was proposed in [14] to drive multiple power MOSFETs with floating grounds in a switched capacitor dc/dc converters. A low-side and high-side resonant gate driver was proposed for a synchronous buck converter in [15] and [16]. An assessment of resonant drive techniques in low power dc/dc converters was presented in [17]. The effects of internal parasitic inductance and the parasitic output capacitance of the driver switches were analyzed focusing on their impact on the SR driver losses in different nonisolated resonant driver topologies [18], [19]. Self-driven nonisolated topologies in [20]–[22] were proposed to reduce the high-gate-drive loss of the SRs. Zero-voltage-switching (ZVS) technology was used to reduce the switching losses in this topology similar to full-bridge converters [23], [24]. Unfortunately, all the aforementioned investigations are generally concentrating on reducing gate-drive losses with the different resonant drivers, but ignore the potential switching loss savings that are much more dominant in megahertz switching power converters.

Compared to resonant gate drivers, current-source drivers (CSDs) are proposed to reduce the dominant switching loss at high-switching frequency (>1 MHz). Since the basic idea of the CSDs is to achieve the switching loss reduction other than the gate energy recovery for the control MOSFETs, the design criteria turns to be different. The dual channel low-side CSD was proposed for the interleaving boost converters in [25]. The advantage of this CSD is that only one inductor is required to drive two power MOSFETs. A continuous current dual channel CSD using bootstrap technique was proposed in [26] and [27] to achieve the switching loss reduction and SR gate energy recovery in a buck converter and its improved version was presented in [28]. However, the disadvantage of the continuous CSDs is the gate-drive currents vary with the duty cycle and the switching frequency, and furthermore, the inductance value is high (typically, 1 μH at the switching frequency of 1 MHz). In addition, the switching frequency variation will impact on the inductance value of the continuous CSDs. A discontinuous CSD was proposed in [29], however, in this drive circuit, one drive switch could not use bootstrap technology, since there is no bootstrap

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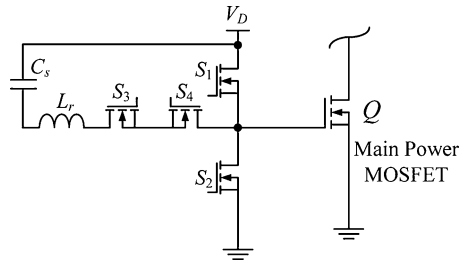


Fig. 1. Proposed discontinuous CSD.

current path. Moreover, this CSD still concentrates on gate energy recovery. A discontinuous CSD proposed in [30] and [31] is able to achieve significant switching loss reduction. The key to this type of CSDs is to control of the driver switches to generate discontinuous inductor-current waveforms enabling the peak portion of the inductor current to be used to charge/discharge the power MOSFET gate as a near constant current source. Based on an accurate analytical loss model, a significant reduction of the switching transition time and the switching loss was verified for a 1 MHz buck converter theoretically and experimentally in [32].

The objective of this paper is to present a new CSD with discontinuous inductor current. Compared to other CSDs proposed in previous work, the most important advantage of the proposed CSD is the small inductance (typically, 20 nH at 1 MHz switching frequency). Section II presents the proposed CSD and its principle of operation. Section III presents the loss analysis and design procedure. Section IV contains the experimental results and discussion. Section V provides a brief conclusion.

II. Proposed CSD and its Principle of Operation

The proposed CSD is illustrated in Fig. 1. It consists of four drive switches S_1–S_4, a small inductor L_r, and a series capacitor C_s. V_D is the gate-drive voltage. In the analysis, it is assumed that the same MOSFETs (n-channel) are used for S_1–S_4. S_1–S_4 are controlled to allow the inductor current to be discontinuous and the power MOSFET can be turned ON or OFF with a nonzero precharge current. During charging or discharging of the power MOSFET, the excess stored energy in the inductor is allowed to return to the series capacitor C_s and to the drive voltage source.

Fig. 2 illustrates the control gating signals, inductor current i_{L_r}, gate current i_G, and power MOSFET gate-to-source voltage v_{GS}. The key waveforms to note are: 1) S_1 and S_2 are switched out of phase with complimentary control to drive Q; 2) the inductor current i_{L_r} is discontinuous to minimize conduction loss; and 3) the gate-drive current i_G is relatively constant during turn ON and turn OFF transition, which achieves fast switching speed of the power MOSFET.

A. Principle of Operation

There are eight switching modes in one switching period. The operation of the circuit is explained in the following paragraphs. The equivalent circuits of turn ON transition are illustrated in Fig. 3(a)–(d). D_1–D_4 are the body diodes of S_1–S_4.

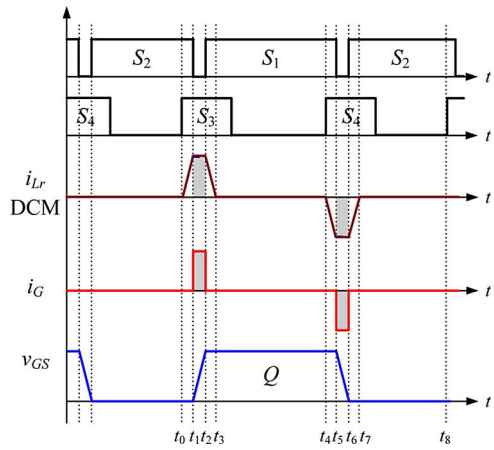


Fig. 2. Key waveforms of the proposed CSD. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$. (c) $[t_2, t_3]$. (d) $[t_3, t_4]$.

C_1 and C_2 are the intrinsic drain-to-source capacitors of S_1 and S_2. C_{gs} is the intrinsic gate-to-source capacitor of the main power MOSFET Q. The switching transitions of charging and discharging C_{gs} are during the intervals of $[t_1, t_2]$ and $[t_5, t_6]$, respectively, as shown in Fig. 2. The peak current i_G during $[t_1, t_2]$ and $[t_5, t_6]$ are nearly constant during the switching transition, which ensures fast charging and discharging the gate capacitance of Q, including the miller capacitor. When the inductor current charges or discharges gate capacitance, since the CSD inductor is in series with the gate parasitic inductance, the parasitic gate inductance can be absorbed. In order to simplify the analysis of the equivalent circuits, the gate parasitic inductance is not shown there. Initially, it is assumed that the power MOSFET is in the OFF state before time t_0.

1) *Mode 1 [t_0, t_1] [see Fig. 3(a)]:* Prior to t_0, S_2 is ON and the gate of Q is clamped to ground. At t_0, S_3 turns ON [with zero-current-switching (ZCS)] allowing the inductor current i_{L_r} to ramp up through D_4. The current path during this interval is C_s–L_r–S_3–D_4–S_2. This interval is the inductor current precharge interval and it ends at time t_1, which is a predetermined time set by the user. Since S_2 is in the ON state, the gate of Q is always clamped low.
2) *Mode 2 [t_1, t_2] [see Fig. 3(b)]:* At t_1, S_2 is turned OFF, which allows the inductor current to begin to charge the gate capacitor C_{gs}. i_{L_r} charges C_2 plus the input capacitor C_{gs} and discharges C_1 simultaneously. Due to C_1 and C_2, S_2 is zero-voltage turn OFF. The inductor current can be regarded as a current source during this interval.
3) *Mode 3 [t_2, t_3] [see Fig. 3(c)]:* At t_2, v_{c2} rises to V_D and v_{c1} decays to zero. The body diode D_1 conducts and S_1 turns ON under zero-voltage condition. The inductor current continues to conduct through the path C_s–L_r–S_3–D_4–S_1. This interval continues for a short duration until t_3. During this interval, the gate of Q is clamped to the drive voltage V_D. This interval ends when the inductor current reaches zero at t_3. It is noted that it is during this interval when the stored energy in the inductor is returned to C_s. Also during this interval, the inductor voltage has

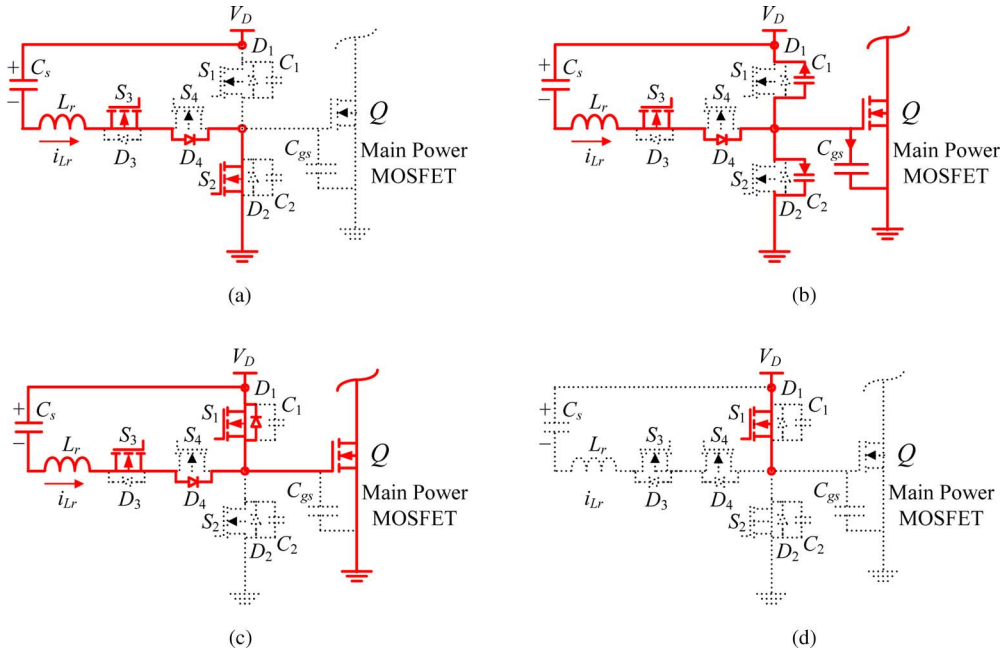


Fig. 3. Equivalent circuits: turn ON intervals. (a) $[t_4, t_5]$. (b) $[t_5, t_6]$. (c) $[t_6, t_7]$. (d) $[t_7, t_8]$.

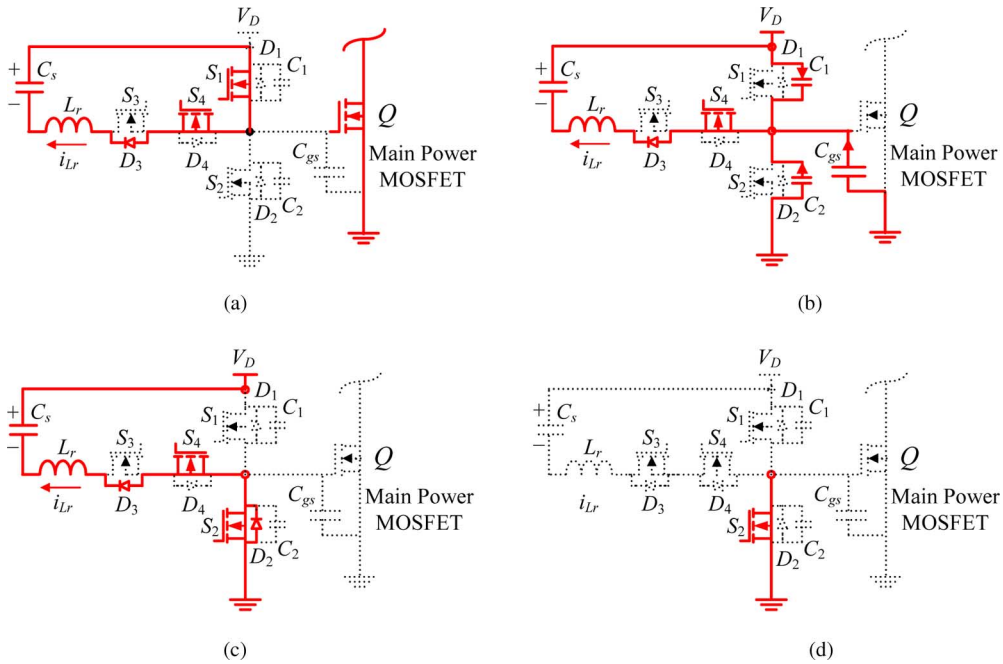


Fig. 4. Equivalent circuits: turn OFF intervals.

become reversely biased, so the inductor current quickly ramps down towards zero.

4) *Mode 4 [t_3, t_4] [see Fig. 3(d)]:* At t_3, D_4 turns OFF (with ZCS) and the inductor current is zero. During this interval, the gate of Q remains clamped high. This interval ends at t_4 when the precharged interval for the turn OFF cycle begins as dictated by the pulsewidth modulation (PWM) control signals.

The equivalent circuits of turn OFF intervals are illustrated in Fig. 4(a)–(d).

5) *Mode 5 [t_4, t_5] [see Fig. 4(a)]:* At t_4, S_4 turns ON (with ZCS). Since S_1 was previously ON, the inductor current i_{L_r} begins to ramp negative through the path C_s–S_1–S_4–D_3–L_r. The energy charge the inductor is provided by C_s. During this interval, the gate of Q remains clamped to V_D. This interval ends at t_5.

6) *Mode 6 [t_5, t_6] [see Fig. 4(b)]:* At t_5, S_1 is turned OFF, which allows the inductor current to begin to discharge the gate capacitor C_{gs}. i_{L_r} discharges C_2 plus the input capacitor C_{gs} and charges C_1 simultaneously. Due to C_1

and C_2, S_1 is zero-voltage turn OFF. The inductor current continues to ramp negative from the precharged level.

7) *Mode 7 [t_6, t_7] [see Fig. 4(c)]:* At t_6, v_{c1} rises to V_D and v_{c2} decays to zero. The body diode D_2 conducts and S_2 turns ON under zero-voltage condition. The inductor current continues to conduct through the path C_s–L_r–D_3–S_4–S_2. This interval continues for a short duration until t_7. During this interval, the inductor voltage becomes reversely biased, so the inductor current quickly ramps down towards zero. It is noted that it is during this interval when the stored energy in the inductor is returned to the drive voltage source. During this interval, the gate of Q is clamped low. This interval ends when the inductor current reaches zero at t_7.
8) *Mode 8 [t_7, t_8] [see Fig. 4(d)]:* At t_7, D_3 turns OFF (with ZCS) and the inductor current is zero. During this interval, the gate of Q_1 remains clamped low. This interval ends at t_8, when the precharged interval for the turn ON cycle begins and the entire process repeats as dictated by the PWM control signal.

B. Gate-Drive Current of the Power MOSFET

The precharge current to turn ON and turn OFF the power MOSFET is decided by the voltage to charge the current-source inductor and the precharge time. For the turn ON current, the voltage to charge the inductor is $(V_D - V_{C_s})$ and the precharge time from t_0 to t_1 (t_{10}) [seen from Fig. 3(a)]. From t_2 to t_3 (t_{32}) [seen from Fig. 3(c)], the inductor voltage across the inductor is V_{C_s} and the energy stored in the inductor is returned to C_s, until the inductor current ramps down toward zero.

From the volt–second balance condition across the inductor, following equation should be satisfied:

$$(V_D - V_{C_s})t_{10} = V_{C_s}t_{32} \tag{1}$$

where V_D is the drive voltage and V_{C_s} is the dc voltage across the capacitor.

From (1), assuming $t_{10} = t_{32}$, the dc voltage across the series capacitor is self-regulated as follows:

$$V_{C_s} = \frac{V_D}{2}. \tag{2}$$

Referring to Fig. 3(a), the inductor current charges the series capacitance C_s during the precharge interval t_{10}. The voltage ripples over C_s during t_{10} is as follows:

$$\Delta V_{C_s} = \frac{1}{C_s}\int_0^{t_{10}} \frac{V_D - V_{C_s}}{L_r} t dt = \frac{V_D}{4C_sL_r}t_{10}^2. \tag{3}$$

In order to achieve a constant ramp rate during t_{10}, the voltage ripple ΔV_{C_s} should be considered. Substituting (2) to (3), the value of C_s should meet

$$C_s \geq \frac{V_D}{4\Delta V_{C_s}L_r}t_{10}^2. \tag{4}$$

For example, for $\Delta V_{C_s} = 0.25$ V (5% of V_D), $L_r = 22$ nH, $V_D = 5$ V, and $t_{10} = 15$ ns, then C_s should be larger than 0.05 μF. Compared to other continuous CSDs with the capacitance of around 1 μF, the capacitance of this proposed CSD is much reduced. This is because the discontinuous CSD has much less time for the inductor current to charge the capacitance compared to the continuous CSDs, so that for the same voltage ripples, less capacitance is needed for the discontinuous CSD.

Referring to Fig. 3(a), the precharge current to turn ON the power MOSFET is as follows:

$$I_{G\_ON} = \frac{V_D - V_{C_s}}{L_r}t_{10}. \tag{5}$$

Substituting (2) to (5), the turn ON current is as follows:

$$I_{G\_ON} = \frac{V_D}{2L_r}t_{10}. \tag{6}$$

Similarly, referring to Fig. 4(a), the precharge current to turn OFF the power MOSFET is as follows:

$$I_{G\_OFF} = \frac{V_{C_s}}{L_r}t_{54} = \frac{V_D}{2L_r}t_{54}. \tag{7}$$

From (6) and (7), by changing precharge time t_{10} and t_{54}, the turn ON gate current and turn OFF gate current can be decided. The tolerance of the inductor can be less than 10%. Considering the variation of the inductance, the precharge time can be adjusted to obtain the required gate-drive current. In the experiment, since we use the logic gates to achieve delay time (for Altera Max II EPM240 complex program logic device (CPLD), 30 gates give 10 ns delay), the delay time of the control signals, such as precharge time and dead time can be adjusted precisely and conveniently, owing to the programmable capability of CPLD. The tolerance of the delay in digital circuit is usually small and in the range of 100 ps, which will not introduce large error.

It is also noted that compared to the discontinuous CSD in [30], since the actual voltage over the inductor is reduced by half as V_D/2, for the same precharge time and gate-drive current, the proposed CSD can further reduce the inductance value by half.

C. Benefits of the Proposed CSD

The advantages of the new CSD are highlighted as follows.

1) Small current-source inductance: One of the most important advantages of the proposed CSD is the small inductance. The resonant gate drive proposed in [7], [8], [13], [14], and the CSDs in [25] and [26] have continuous inductor current. The advantages are that they normally need two drive switches for a single MOSFET and need less control circuitry, and these drive switches can also achieve ZVS. However, the disadvantages are that they require large resonant inductance values (typically, 1 μH at the switching frequency of 1 MHz), and thus have high-circulating current and high-conduction loss.

The advantage of the proposed CSD is very low inductance value, only 20 nH at the switching frequency of 1 MHz. This is a significant reduction of the inductance value. For example, if Coilcraft surface mount (SMT) DS3316 [33] is chosen as 1 μH inductor, while Coilcraft SMT 1812SMS [34] is chosen as 22 nH inductor, and the footprint reduction is as much as 90%. This yields a significant space saving on the Motherboard. The disadvantage is that the proposed CSD needs four drive switches for a single MOSFET. However, due to the discontinuous induc-

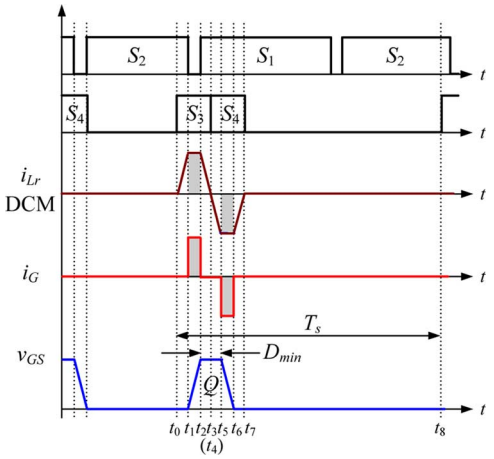


Fig. 5. Key waveforms with minimum duty cycle.

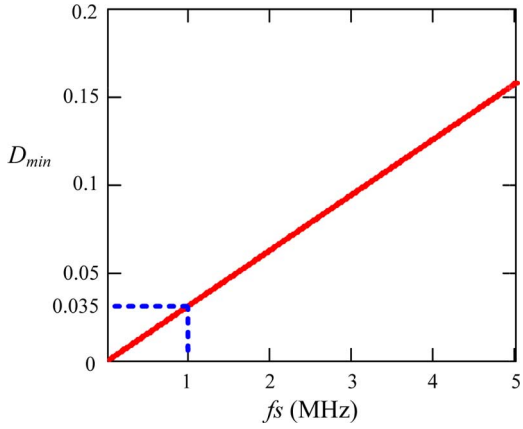


Fig. 6. Minimum duty cycle versus the switching frequency.

tor current, these four driver switches can use the MOSFETs with relatively high $R_{DS(\mathrm{ON})}$.

2) Significant reduction of the switching transition time and switching loss: The disadvantages of the resonant gate drivers in [1], [8], [9], [12], and [15] are slow turn ON or turn OFF transition, which increases both conduction and switching losses in the power MOSFET due to the gate-drive current beginning at zero current. The key idea of the proposed CSD is to control the four drive switches to create a constant current source to drive the main power MOSFETs. During the switching transition $[t_1, t_2]$ and $[t_5, t_6]$ (see Fig. 2). The advantage of the proposed CSD is that it uses the precharge inductor current to drive the control MOSFET and absorbs the parasitic inductance. This reduces the propagation impact of the parasitics during the switching transition, which leads to a reduction of the switching transition time and switching loss. At the same time, the discontinuous current does not increase the circulating loss compared to continuous CSDs.

3) Gate energy recovery: The stored energy in the inductor is returned to the series capacitor C_s during $[t_2, t_3]$ and is returned to the drive voltage source during $[t_6, t_7]$ (see Fig. 2). One benefit of the gate energy recovery capability is that higher gate-drive voltage can be used to further reduce $R_{DS(\mathrm{ON})}$ conduction loss.

4) Wide range of duty cycle and switching frequency: In a high-frequency buck converter, the duty cycle is required to change fast during a transient event. At the same time, in order to improve the efficiency in a wide-load range, the switching frequency of a buck converter may need to vary according to the load condition. The duty cycle range and switching frequency are analyzed as follows.

As seen from Fig. 2, when the duty cycle reduces, the time from t_4 to t_3 (t_{43}) reduces accordingly, until Fig. 2 changes into Fig. 5, which illustrates the waveforms of the minimum duty cycle.

From Fig. 5 and (2), the energy recovery time t_{32} is as follows:

$$t_{32} = \frac{I_{G\_\mathrm{ON}} L_r}{V_{C_s}} = \frac{I_{G\_\mathrm{ON}} L_r}{V_D/2} = \frac{2I_{G\_\mathrm{ON}} L_r}{V_D}. \tag{8}$$

From Fig. 5 and (8), the minimum $t_{\min}$ is as follows:

$$t_{\min} = t_{32} + t_{54} = \frac{2I_{G\_\mathrm{ON}} L_r}{V_D} + t_{54} \tag{9}$$

where t_{54} is the precharge time for turn OFF current.

Therefore, from (9), the minimum duty cycle $D_{\min}$ is as follows:

$$D_{\min} = \frac{t_{\min}}{T_s} = \frac{2I_{G\_\mathrm{ON}} L_r}{V_D T_s} + \frac{t_{54}}{T_s} = \left(\frac{2I_{G\_\mathrm{ON}} L_r}{V_D} + t_{54}\right) f_s \tag{10}$$

where f_s is the switching frequency.

As an example, Fig. 6 shows the minimum duty cycle as the function of the switching frequency, where $I_{G\_\mathrm{ON}} = 2.3$ A, $L_r = 22$ nH, $V_D = 5$ V, and $t_{54} = 15$ ns. It is observed that $D_{\min}$ increases when the switching frequency increases, and particularly, at $f_s = 1$ MHz, $D_{\min}$ is 0.035, which is small enough for most applications.

From (10), if we have the minimum duty cycle requirement as $D_{\min\_\mathrm{req}}$, the switching frequency should meet

$$f_s \le \frac{D_{\min\_\mathrm{req}}}{(2I_{G\_\mathrm{ON}} L_r)/V_D + t_{54}}. \tag{11}$$

As seen from Fig. 2, when the duty cycle increases, the time from t_8 to t_7 (t_{87}) reduces accordingly, until Fig. 2 changes into Fig. 7, which illustrates the waveforms of the maximum duty cycle.

From Fig. 7, the turn ON time t_{21} is as follows:

$$t_{21} = \frac{C_{gs} V_D}{I_{G\_\mathrm{ON}}}. \tag{12}$$

From (2), the turn OFF time t_{65} is as follows:

$$t_{65} = \frac{C_{gs} V_D}{I_{G\_\mathrm{OFF}}}. \tag{13}$$

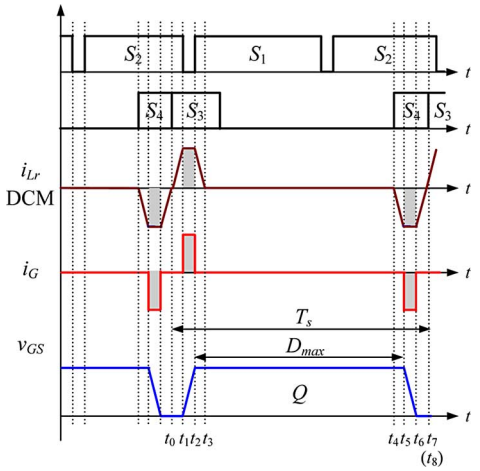


Fig. 7. Key waveforms with maximum duty cycle.

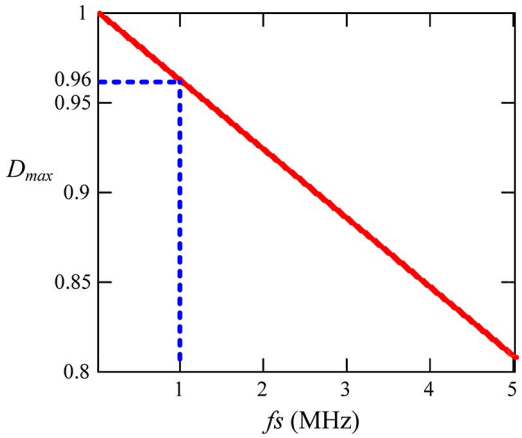


Fig. 8. Maximum duty cycle versus the switching frequency.

Referring to Fig. 5 and from (2), the energy recovery time t_{76} is as follows:

$$t_{76} = \frac{2I_{G\_\mathrm{OFF}}L_r}{V_D}. \tag{14}$$

From (12)–(14), the maximum time $t_{\max}$ is as follows:

$$t_{\max} = T_s - t_{10} - t_{21} - t_{65} - t_{76} = T_s - t_{10} - \frac{C_{gs}V_D}{I_{G\_\mathrm{ON}}} - \frac{C_{gs}V_D}{I_{G\_\mathrm{OFF}}} - \frac{2I_{G\_\mathrm{OFF}}L_r}{V_D}. \tag{15}$$

Therefore, from (15), the maximum duty cycle $D_{\max}$ is as follows:

$$D_{\max} = \frac{t_{\max}}{T_s} = 1 - \frac{t_{10}}{T_s} - \frac{C_{gs}V_D}{I_{G\_\mathrm{ON}}T_s} - \frac{C_{gs}V_D}{I_{G\_\mathrm{OFF}}T_s} - \frac{2I_{G\_\mathrm{OFF}}L_r}{V_D T_s} = 1 - \left(t_{10} + \frac{C_{gs}V_D}{I_{G\_\mathrm{ON}}} + \frac{C_{gs}V_D}{I_{G\_\mathrm{OFF}}} + \frac{2I_{G\_\mathrm{OFF}}L_r}{V_D}\right) f_s. \tag{16}$$

As an example, Fig. 8 shows the maximum duty cycle as the function of the switching frequency, where for $I_{G\_\mathrm{ON}} = I_{G\_\mathrm{OFF}} =$ 2.3 A, $C_{gs} = 1.6$ nF, $L_r = 22$ nH, $V_D = 5$ V, and $t_{10} = 15$ ns. It is observed that $D_{\max}$ decreases when the switching frequency

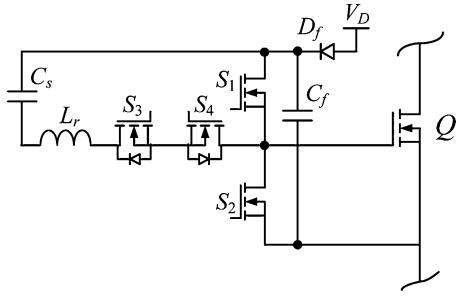


Fig. 9. Proposed high-side CSD.

increases, and particularly, at $f_s = 1$ MHz, $D_{\max}$ is 0.96, which is large enough for most application.

From (16), if we have the maximum duty cycle requirement as $D_{\max\_\mathrm{req}}$, the switching frequency should also meet

$$f_s \le \frac{1 - D_{\max\_\mathrm{req}}}{t_{10} + C_{gs}V_D/I_{G\_\mathrm{ON}} + C_{gs}V_D/I_{G\_\mathrm{OFF}} + 2I_{G\_\mathrm{OFF}}L_r/V_D}. \tag{17}$$

As a conclusion, the proposed CSD can operate correctly with the minimum duty cycle of 0.035 and maximum duty cycle of 0.96 with the 1 MHz switching frequency; meantime, the advantages of the fast switching speed and gate energy recovery can still be maintained. For some extreme conditions, we can add extra logic circuits to achieve the duty cycle of zero or 100%. Therefore, it is suitable for different types of control and wide operating conditions.

5) High noise immunity: The disadvantage of the resonant gate drivers in [1], [8], [9], [12], [14], and [15] is the inability to actively clamp the power MOSFET gate to the drive voltage during the ON time and/or to ground during the OFF time, which can lead to undesired false triggering of the power MOSFET gate, i.e., lack of *Cdv/dt* immunity.

The advantage of the proposed CSD is that the gate terminal of the power MOSFETs are clamped to either the drive voltage via a low impedance path [S_1 with fairly small $R_{DS(\mathrm{ON})}$] or the source terminal via S_2. This offers high noise immunity and leads to the alleviation of *dv/dt* effect.

D. Proposed High-Side CSD and Hybrid Gate-Drive Scheme

Fig. 9 illustrates the proposed high-side CSD for nonground referenced power MOSFET. It uses a bootstrap circuit consisting of a diode D_f and a bootstrap capacitor C_f. This CSD can be used to the control MOSFET in a buck converter to achieve fast switching and reduced switching loss.

Fig. 10 illustrates another version of the high-side CSD using C_{s1} and C_{s2} in series as the bootstrap capacitor, where C_{s1} and C_{s2} also serve as the bootstrap capacitors.

Fig. 11 shows the proposed hybrid gate-drive scheme for a buck converter. For the control MOSFET Q_1, the proposed high-side CSD is used to achieve the switching loss reduction. For the SR Q_2, the conventional voltage-source driver is used for low cost and simplicity. PWM_SR is the signal fed into the voltage-source driver.

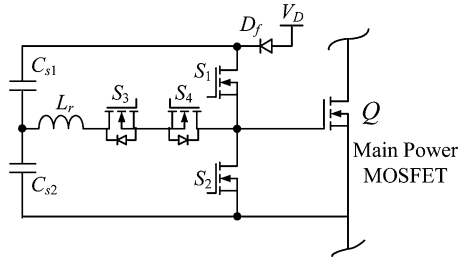


Fig. 10. Proposed high-side CSD using series capacitors.

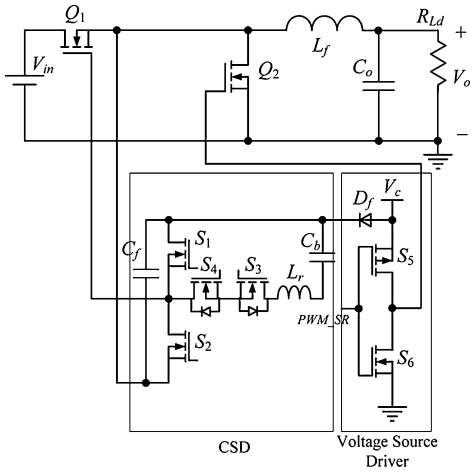


Fig. 11. Buck converter with proposed discontinuous CSD.

III. Loss Analysis and Design Procedure

Based on the principle of operation, the loss analysis for the proposed CSD is presented in this section. This provides design guideline for the proposed CSD.

A. Loss Analysis

1) Conduction Loss: Fig. 12 illustrates the power MOSFET gate voltage and gate-drive current waveforms during the turn ON interval. The current paths are also listed under the waveforms.

1) *Interval [t_0, t_1] [see Fig. 3(a)]:* The inductor current path is S_3–D_4–S_2.

The rms current is as follows:

$$I_{\mathrm{rms}\_t_{10}} = I_{G\_\mathrm{ON}}\sqrt{\frac{t_{10}f_s}{3}} \tag{18}$$

where I_{G_ON} is the precharge turn ON current, which can be calculated from (5).

The average value is as follows:

$$I_{\mathrm{Avg}\_t_{10}} = \frac{I_{G\_\mathrm{ON}}}{2}t_{10}f_s. \tag{19}$$

The total conduction loss is as follows:

$$P_{t_{10}} = 2I^2_{\mathrm{rms}\_t_{10}}R_{DS(\mathrm{ON})} + I_{\mathrm{Avg}\_t_{10}}V_F. \tag{20}$$

From (18)–(20), P_{t10} becomes

$$P_{t_{10}} = \frac{2}{3}I^2_{G\_\mathrm{ON}}t_{10}f_sR_{DS(\mathrm{ON})} + \frac{1}{2}I_{G\_\mathrm{ON}}V_Ft_{10}f_s \tag{21}$$

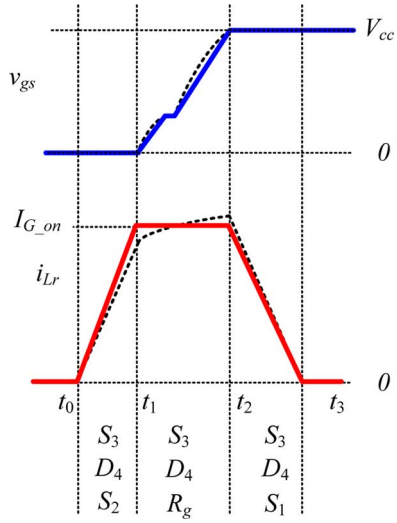


Fig. 12. Detailed inductor current and power MOSFET gate voltage waveforms during the turn ON interval.

where $R_{DS(\mathrm{ON})}$ is the ON-resistance of S_1–S_4, assuming S_1–S_4 are same and V_F is the forward voltage of the body diode.

2) *Interval [t_1, t_2] [see Fig. 3(b)]:* The inductor current path is S_3–R_g–D_4 to charge gate capacitor C_{gs}.

The rms current is as follows:

$$I_{\mathrm{rms}\_t_{21}} = I_{G\_\mathrm{ON}}\sqrt{t_{21}f_s}. \tag{22}$$

The average value is as follows:

$$I_{\mathrm{Avg}\_t_{21}} = I_{G\_\mathrm{ON}}t_{21}f_s. \tag{23}$$

The total conduction loss is as follows:

$$P_{t_{21}} = I^2_{\mathrm{rms}\_t_{21}}R_{DS(\mathrm{ON})} + I^2_{\mathrm{rms}\_t_{21}}R_g + I_{\mathrm{Avg}\_t_{21}}V_F. \tag{24}$$

From (22)–(24), following equation is obtained:

$$P_{t_{21}} = I^2_{\mathrm{rms}\_t_{21}}R_{DS(\mathrm{ON})} + I^2_{\mathrm{rms}\_t_{21}}R_g + I_{\mathrm{Avg}\_t_{21}}V_F \tag{25}$$

where $R_{DS(\mathrm{ON})}$ is the ON-resistance of S_1–S_4, assuming S_1–S_4 are same, R_g is the gate mesh resistance, and V_F is the diode forward voltage.

3) *Interval [t_2, t_3] [see Fig. 3(c)]:* The inductor current path is S_3–D_4–S_1.

The rms current is as follows:

$$I_{\mathrm{rms}\_t_{32}} = I_{G\_\mathrm{ON}}\sqrt{\frac{t_{32}f_s}{3}}. \tag{26}$$

The average value is as follows:

$$I_{\mathrm{Avg}\_t_{32}} = \frac{I_{G\_\mathrm{ON}}}{2}t_{32}f_s. \tag{27}$$

The total conduction loss is as follows:

$$P_{t_{32}} = 2I^2_{\mathrm{rms}\_t_{32}}R_{DS(\mathrm{ON})} + I_{\mathrm{Avg}\_t_{32}}V_F. \tag{28}$$

From (26)–(28), following equation is obtained:

$$P_{t_{32}} = \frac{2}{3}I^2_{G\_\mathrm{ON}}t_{23}f_sR_{DS(\mathrm{ON})} + \frac{1}{2}I_{G\_\mathrm{ON}}V_Ft_{23}f_s. \tag{29}$$

To simplify the analysis, it can be assumed that the turn ON and turn OFF states of operation are identical. Therefore, under

this assumption, the total conduction loss in the proposed CSD is two times the sum of $P_{t_{10}}$, $P_{t_{21}}$, and $P_{t_{32}}$, as given as follows:

$$P_{\text{cond}} = (P_{t_{10}} + P_{t_{21}} + P_{t_{32}})2. \tag{30}$$

2) Current-Source Inductor Loss: The copper loss of the inductor winding is as follows:

$$P_{\text{copper}} = R_{\text{ac}} I^2_{L_r\_\text{rms}} \tag{31}$$

where R_{ac} is the ac resistance of the inductor winding and $I_{L_r\_\text{rms}}$ is the rms value of the inductor current, which can be calculated as follows:

$$I_{L_r\_\text{rms}} = \sqrt{2(I^2_{\text{rms}\_t_{10}} + I^2_{\text{rms}\_t_{21}} + I^2_{\text{rms}\_t_{32}})}. \tag{32}$$

Core loss of the inductor should be also included. The core loss can be obtained by standard core loss estimation methods and should be small in comparison to the other loss components. If air core inductors are used, the core loss is zero.

3) Gate-Drive Loss: The gate-drive loss of S_1–S_4 is as follows:

$$P_{\text{gate}} = 4Q_{g\_s}V_{gs\_s}f_s \tag{33}$$

where Q_{g_s} is the total gate charge of a drive switch and V_{gs_s} is the drive voltage, which is typically 5 V.

B. Design Example

1) Optimal Design for Buck Converter: For the given application, in order to achieve fast switching speed, the gate-drive current (precharge current) should be chosen by the designer properly. The design tradeoff is between switching speed, which translates into reduced switching loss and gate-drive loss. Higher gate charge current leads to lower switching loss, but results in greater conduction loss in the CSD. As seen from Fig. 2, the peak current $I_{L_{r\_\text{pk}}}$ of the resonant inductor L_r is regarded as the current source magnitude I_G. Therefore, the higher $I_{L_{r\_\text{pk}}}$ is, the shorter of switching transition is, thus more switching loss can be saved. However, higher $I_{L_{r\_\text{pk}}}$ will result in a larger rms value of the inductor circulating current i_{L_r}, since the waveform of i_{L_r} is triangular, which increases the resistive circulating loss in the drive circuit and decreases the gate energy recovery efficiency. Therefore, it is critical to decide $I_{L_{r\_\text{pk}}}$ (i.e., I_G) properly, so that the maximum loss saving can be achieved.

The optimal design is applied to the buck converter with the hybrid drive scheme in Fig. 11. In [32], the switching loss model with the CSD and optimal method proposed. The basic idea is to find the optimal solution on the basis of the object function that adds the switching loss and the CSD circuit loss together. The object function should be a U-shape curve as function of the drive current I_G, and the optimization solution is simply located at the lowest point of the curve.

Based on the same idea, Fig. 13 illustrates the switching loss $p\_{\text{switching loss}}$, the CSD circuit loss $p\_{\text{CSD circuit}}$, and the objective function $F(I_G)$ as function of the gate-drive current I_G, respectively. The specifications of the buck converter are: $V_{\text{in}} = 12$ V, $V_o = 1.3$ V, $I_o = 30$ A, $V_c = 5$ V, and $f_s = 1$ MHz; control MOSFET Q_1: Si7386DP; Q_2: IRF6691 and $L_f = 330$ nH.

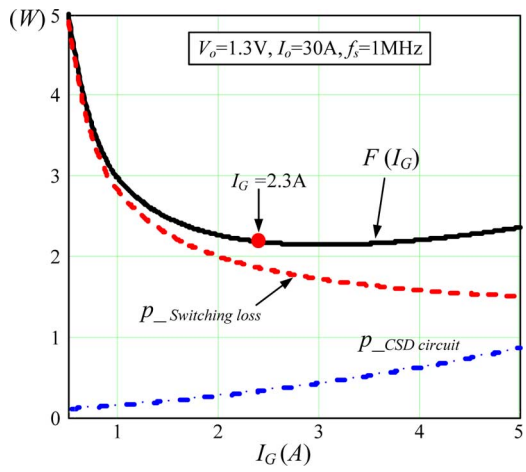


Fig. 13. Objective function $F(I_G)$ as function of current I_G.

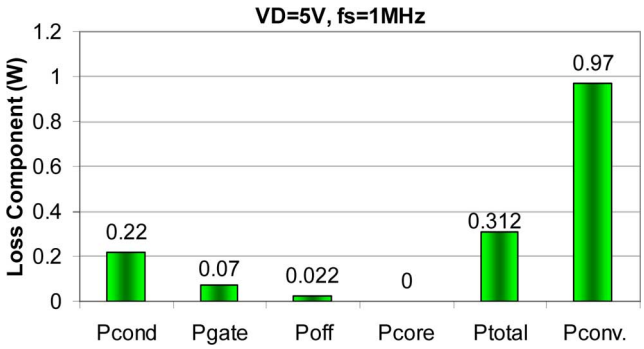


Fig. 14. Loss breakdown of the proposed CSD and total loss comparison with the conventional voltage-source driver.

In Fig. 13, it is observed that $F(I_G)$ is a U-shaped curve, and therefore, the optimization solution can be found at the lowest point of the curve. In this case, the gate-drive current I_G is chosen as 2.3 A. It is noted that the bottom of the U-shape is flat. In other words, when I_G changes from 2 to 3 A, the power loss does not change much.

Once the gate charge current is chosen, the precharge time can be determined accordingly. In order to minimize the delay in the control loop, the precharge time t_{10} should be small. For 1 MHz switching frequency, the precharge time t_{10} is typically 15 ns (2% of the switching period). Considering the variation of the inductance, the precharge time needs be adjusted to achieve desired gate charge current.

From (6), (34) is obtained to calculate the required inductor value

$$L_r = \frac{t_{10}}{2}\frac{V_D}{I_G}. \tag{34}$$

For $t_{10} = 15$ ns, $V_D = 5$ V, and $I_G = 2.3$ A, the inductor value can be chosen as 22 nH.

2) Gate Energy Recovery for SRs: The loss analysis of the CSD circuit in Section III is also used to verify the gate energy recovery of the CSD. Fig. 14 shows the loss breakdown of the proposed CSD with the parameters in Table I. It is noted that

TABLE I
CSD DESIGN PARAMETERS

Circuit Parameters	
Switching Frequency, f_s	1MHz
Gate Drive Voltage, V_D	5V
MOSFET	**IRF6691 (Two paralleled)**
Total Gate Charge@V_{gs}=5V	58nC
Internal Gate Resistance, R_g	1Ω
Driver Switches S_1-S_2	**FDN335**
Diode Forward Voltage, V_F	0.7V
On Resistance $R_{DS(on)}$	70mΩ
Total Gate Charge@V_{gs}=5V:	3.5nC
Driver Inductor L_r	**1812SMS-22**
Inductor Value L_r	22nH
Driver Inductor Resistance	4.2mΩ

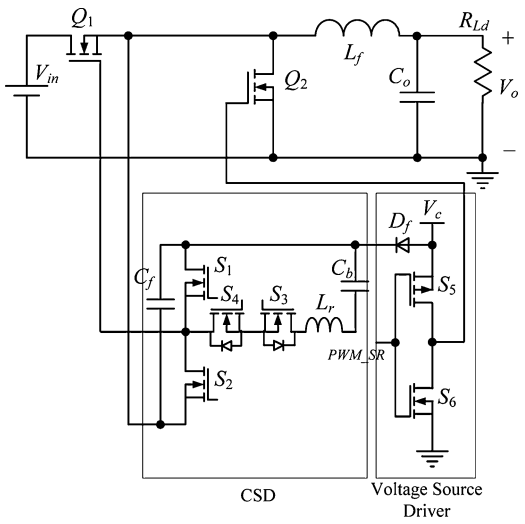


Fig. 15. Proposed discontinuous CSD diagram in the experiment.

compared to the conventional voltage-source driver, the total gate drive loss is reduced by 67.8% with the proposed CSD.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

In order to verify the advantages of the proposed CSD circuit, two experimental tests have been made. The first one is used to verify the switching loss reduction, and the second one is used to verify the gate energy recovery capability.

A. Switching Loss Reduction With the Proposed High-Side CSD

The first experiment is to verify the switching loss reduction with the high side CSD for a 12 V input buck converter. The circuit diagram of the experimental prototype is shown in Fig. 15.

The idea to use the proposed CSD is to achieve fast switching speed and reduce the switching loss of the control MOSFET in a buck converter. Conventional voltage-source driver is used for the SR MOSFET for its simplicity, as there is no switching loss for the SR.

The specifications of the buck converter prototype are as follows: input voltage $V_{\rm in} = 12$ V, output voltage $V_o = 1.0$ V–1.5 V, output current $I_o = 30$ A, switching frequency $f_s = 1$ MHz, and gate-driver voltage $V_c = 5$ V. The printed circuit board (PCB) is six-layer with 4 oz copper. The components used in the circuit are listed as follows: Q_1: Si7386DP, Q_2: IRF6691, output filter inductance $L_f = 330$ nH (IHLP-5050CE-01, Vishay), current-source inductor $L_r = 22$ nH (SMT 1812SMS-22 N, Coilcraft), and drive switches S_1–S_4: FDN335.

Photos of the prototype are illustrated in Fig. 16. The driver was built using discrete components and an Altera Max II EPM240 CPLD was used to generate the driver gate signals, as illustrated in Fig. 16(a). SMT inductor is very small as illustrated in Fig. 16(b).

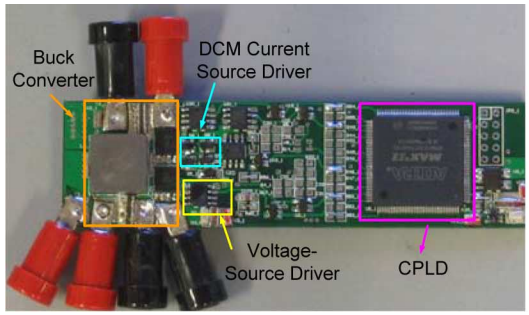
Fig. 17 shows the gate-drive signal for the four drive MOSFETs S_1–S_4 from the CPLD. As seen from Fig. 2, all waveforms agree with the theory. Most notably, the precharge intervals are indicated as 20 ns.

Fig. 18 shows the inductor current i_{L_r} and gate-drive signals v_{GS_Q1} (control MOSFET). Its peak current value is 2.2 A, which is the optimized value of the CSD drive current. The inductor current is discontinuous as expected. During the precharge time, the current ramps up linearly. After the precharge time, the inductor current continues to ramp up, while charging the gate capacitance of the Si7386DP power MOSFET during the turn ON interval. During this interval, the average drive current is approximately 2 A and the power MOSFET voltage charges from 0 V to $V_D = 5$ V. After the power MOSFET turns ON, the inductor current ramps back down to zero, while the inductor energy is returned to drive voltage source.

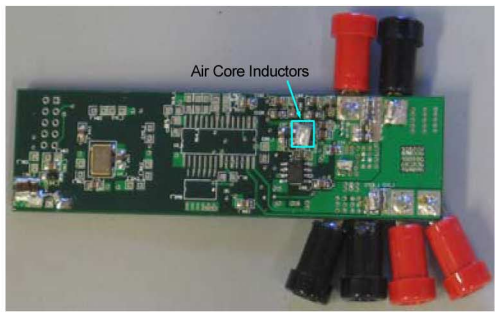
Fig. 19 shows the gate-drive signals v_{GS_Q1} (control MOSFET) and v_{GS_Q2} (SR). It is observed that v_{GS_Q1} is smooth, since the miller charge is removed fast by the constant inductor drive current. Moreover, the total rise time and fall time of v_{GS_Q1} is less than 15 ns, which means fast switching speed is achieved. The dead time between two drive voltages is fixed to avoid shoot-through and is minimized to reduce the SR body diode conduction loss.

Fig. 20 shows the drain-to-source voltage v_{DS_Q2} of the SR at the load current of 25 A. It can be seen from v_{DS_Q2} that the body diode conduction time is small, which reduces the conduction loss and the reverse recovery loss of the body diode. It should be also noted that adaptive control or predictive control of the conventional driver can also be applied to the hybrid gate driver to minimize the body diode conduction time.

A benchmark of a synchronous buck converter with the conventional gate driver was built. The Predictive Gate Drive UCC 27222 from Texas Instruments was used as the conventional voltage driver. Fig. 21 shows the measured efficiency comparison between the hybrid gate driver and the conventional gate driver at 1.3 V output. It is observed that at 25 A, the efficiency is improved from 80.7% to 85.7% (an improvement of 5%) and at 30 A, the efficiency is improved from 77.9% to 84.4% (an improvement of 6.5%).



(a)



(b)

Fig. 16. Photo of the synchronous buck prototype with the hybrid gate driver. (a) Top. (b) Bottom.

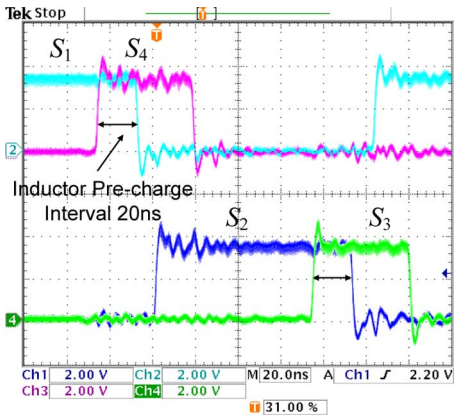


Fig. 17. Gate signals of drive MOSFETs S_1–S_4.

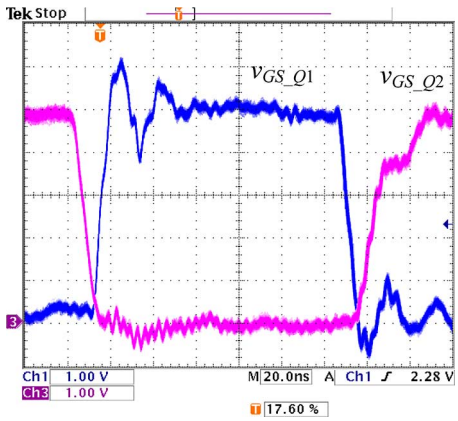


Fig. 19. Gate signals v_{GS_Q1} (control MOSFET) and v_{GS_Q2} (SR).

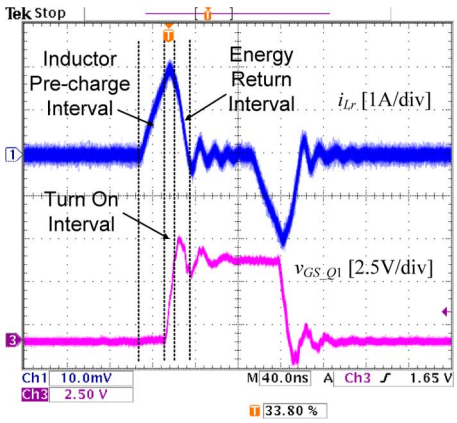


Fig. 18. Inductor current and the gate-to-source voltage at 1 MHz.

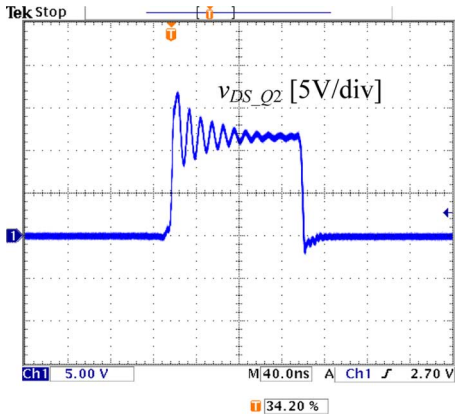


Fig. 20. Drain-to-source voltage v_{DS_Q2} (SR) at load current of 25 A.

Figs. 22–24 show the measured efficiencies for the CSD with different output voltages and load currents at 1 MHz, 750 kHz, and 500 kHz, respectively. It is noted that the same power train parameters and CSD parameters were used for efficiency measurement with different switching frequencies. Since the drive current of the CSD no longer depends on the switching frequencies, the switching loss reduction was still achieved at different conditions. As seen from Fig. 24, at 500 kHz and 1.5 V output voltage, the efficiency reaches 88.1% at 30 A.

Fig. 25 shows the measured efficiency for the CSD at different load currents and $V_o = 1.3$ V when the switching frequency changes. It is observed that at the load current of 30 A, when the switching frequency changes from 1 MHz to 500 kHz, the efficiency is improved from 83.9% to 87% due to the reduction of frequency-dependent losses. The peak efficiency achieves 90.4% at 1.3 V, 15 A, and 500 kHz.

B. Gate Energy Recovery With the Proposed Low-Side CSD for SRs

The second experiment is to verify the gate energy recovery of the proposed CSD. Typically, high-gate-drive voltage helps to reduce the MOSFET $R_{DS(\mathrm{ON})}$ and conduction loss. The SR

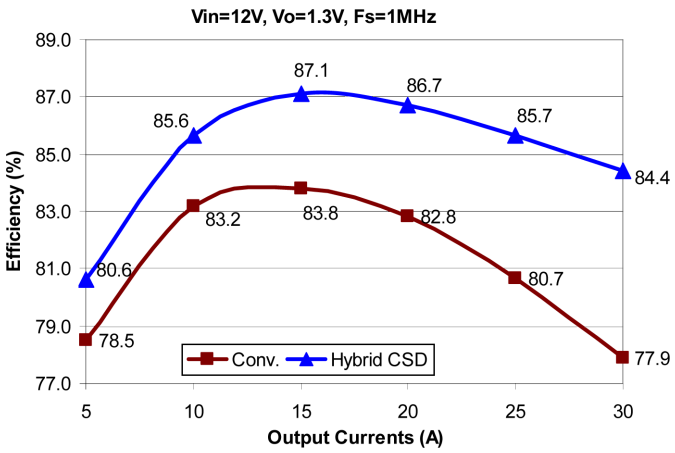


Fig. 21. Efficiency comparison. (Top) Hybrid CSD. (Bottom) Conventional voltage driver (conv.).

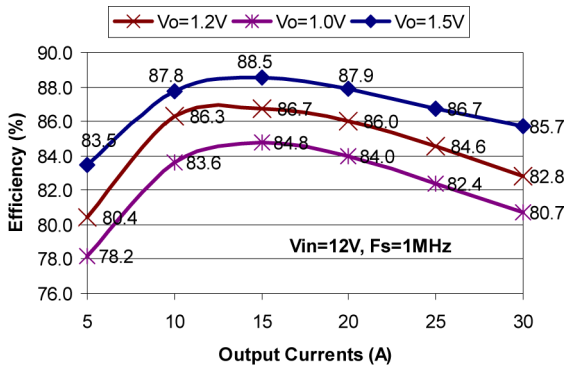


Fig. 22. Efficiency with different output voltages and currents at 1 MHz.

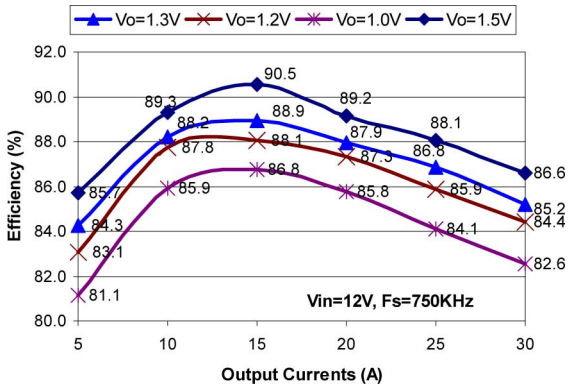


Fig. 23. Efficiency with different output voltages and currents at 750 kHz.

MOSFET usually has high total gate charge. However, it also increases the gate-drive loss. Typically, the gate-drive voltage of 6–7 V gives a good tradeoff between the conduction loss and the gate-drive loss. In addition, in high current application, more SR MOSFETs are often paralleled to reduce $R_{DS(\mathrm{ON})}$ and thus the conduction loss. In this experimental test, the proposed low-side CSD in Fig. 1 is used to drive two paralleled IRF6691 as SRs. The CSD with the same components and parameters is tested. The conventional gate driver chip ISL6208 from Intersil is used for the same SR MOSFETs for comparison [35].

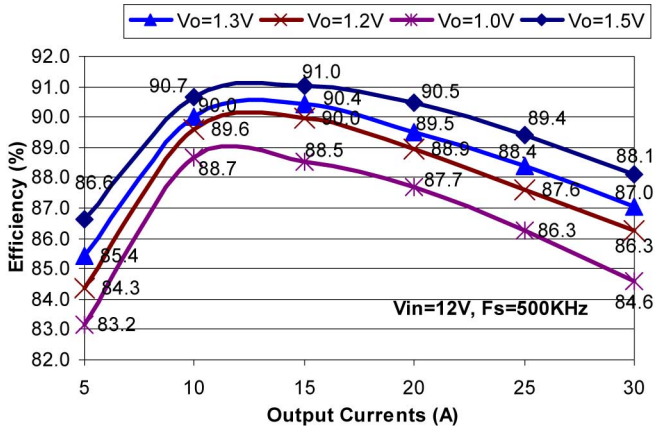


Fig. 24. Efficiency with different output voltages and currents at 500 kHz.

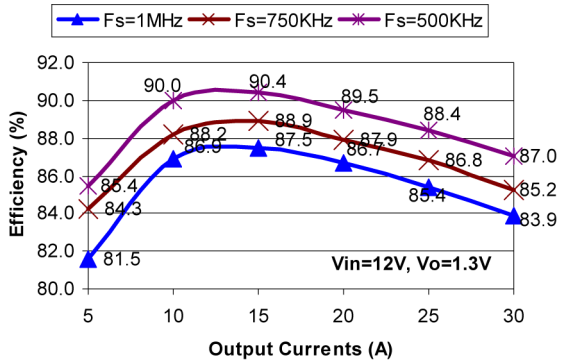


Fig. 25. Efficiency with different currents and switching frequencies at V_o = 1.3 V.

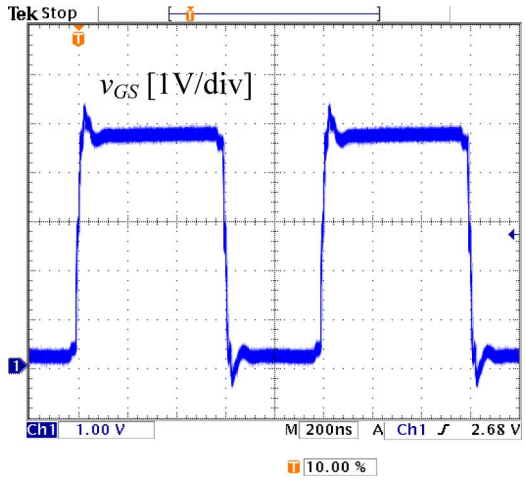


Fig. 26. Gate signals v_{GS} at 1 MHz.

Figs. 26 and 27 illustrate the gate-drive voltages of the SR with the proposed CSD at 1 and 2 MHz, respectively. In both figures, it is observed that the turn ON and turn OFF transition time is less 20 ns, which means that the proposed CSD achieves fast turn ON and turn OFF speed of the SR MOSFET.

The measured losses are listed in Table II. Three different drive voltages of 5, 6, and 7 V are tested under different switching frequency condition. It is observed that when the gate-driver

TABLE II
MEASURED LOSS COMPARISON OF PROPOSED CSD AND CONVENTIONAL (CONV.) VOLTAGE DRIVER

Switching Frequency	V_D=5V			V_D=6V			V_D=7V		
	CSD (W)	Conv. (W)	Δ Loss (W)	CSD (W)	Conv. (W)	Δ Loss (W)	CSD (W)	Conv. (W)	Δ Loss (W)
800kHz	0.28	1.07	0.79	0.40	1.76	1.36	0.56	2.40	1.84
1.0MHz	0.35	1.10	0.75	0.49	1.98	1.49	0.69	2.70	2.01
1.2MHz	0.41	1.30	0.89	0.61	2.06	1.45	0.83	2.80	1.97
1.5MHz	0.52	1.40	0.88	0.75	2.30	1.55	1.02	3.13	2.11
1.8MHz	0.60	1.50	0.90	0.87	2.46	1.59	1.19	3.35	2.16
2.0MHz	0.65	1.62	0.97	0.95	2.60	1.65	1.30	3.54	2.24

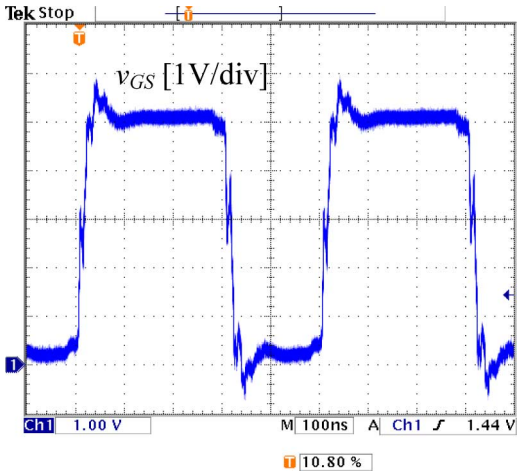


Fig. 27. Gate signals v_{GS} at 2 MHz.

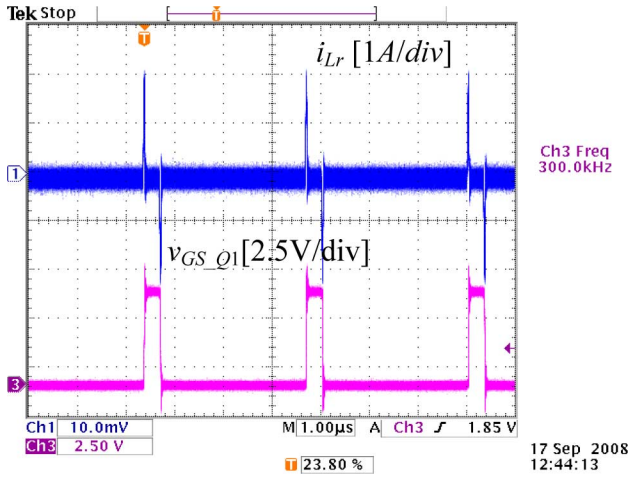


Fig. 28. Inductor current and gate-to-source voltage at 300 kHz.

voltage increases, the loss difference (Δ loss) increases, which means the CSD is more effective when high-gate-drive voltage is applied to reduce $R_{DS(ON)}$ conduction loss. For example, $R_{DS(ON)}$ of IRF6691 is reduced from 2.5 mΩ at $V_{GS} = 5$ V drive voltage to 1.9 mΩ at $V_{GS} = 7$ V (a reduction of 24%) [36]. In Table II, it is noted that with gate-drive voltage $V_D = 7$ V and the switching frequency of 2 MHz, the gate loss reduction with the CSD is as much as 2.24 W, a reduction of 63% with the conventional voltage driver.

C. Wide Operation Range of Duty Cycle and Switching Frequency of the Proposed CSD

The third experiment is to verify the wide operation range of duty cycle and switching frequency of the proposed CSD. For the switching frequency variation, Figs. 28 and 29 illustrate the proposed CSD operates with the switching frequency of 300 and 500 kHz. It is observed that the CSD can operate with different switching frequencies. Because the CSD operates with discontinuous inductor current, the inductor current is only decided by the precharge time even if the switching frequency changes. Therefore, the small inductance can be used in a wide switching frequency range. This is also a great advantage for VR applications in which the switching frequency may be reduced to achieve high efficiency at light load.

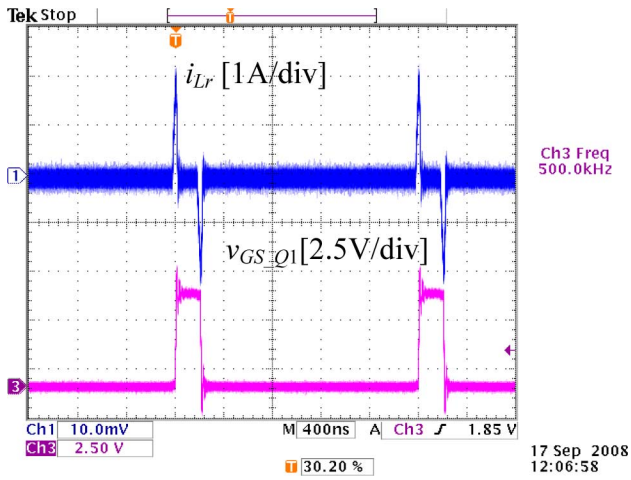


Fig. 29. Inductor current and gate-to-source voltage at 500 kHz.

For the step change of the duty cycle, Figs. 30 and 31 illustrate the duty cycle changes from $D = 0.1$ to 0.8 and from $D = 0.8$ to 0.1, respectively. It is observed that the proposed CSD can response instantaneously when duty cycle has a step change. This is of great benefit for the VR application with fast dynamic response requirement.

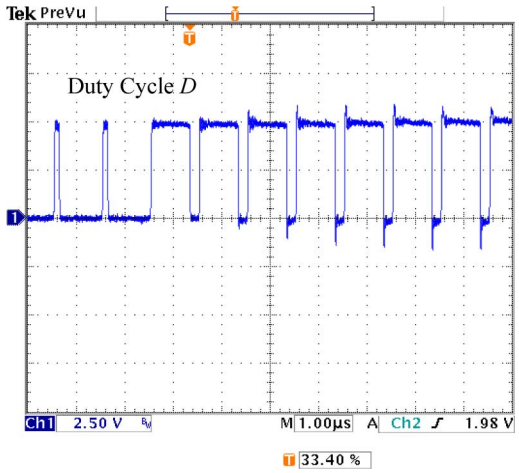


Fig. 30. Gate signals v_{GS_Q1} (control MOSFET) from $D = 0.1$ to 0.8.

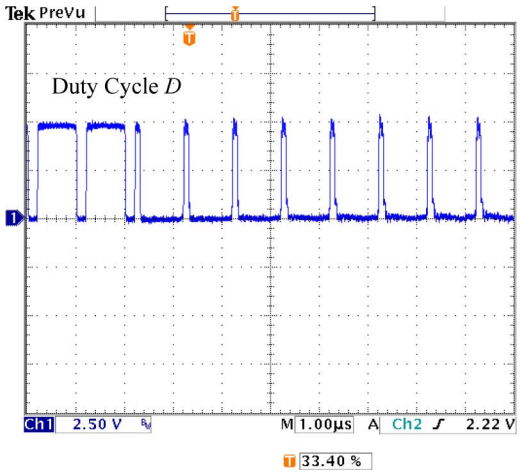


Fig. 31. Gate signals v_{GS_Q1} (control MOSFET) from $D = 0.8$ to 0.1.

V. Conclusion

In this paper, a new discontinuous CSD is proposed. Compared to other CSDs proposed in previous work, the most important advantage of the new CSD is the small inductance (typically, 20 nH at 1 MHz switching frequency). This translates into a footprint reduction of as much as 90%. Other features of the proposed discontinuous CSD are: 1) fast switching speed and reduced switching loss; 2) discontinuous inductor current with low circulating loss; 3) wide range of duty cycle and switching frequency; and 4) high noise immunity.

A hybrid gate-drive scheme for a synchronous buck converter is also proposed to take advantage of the new CSD for a buck converter. The key idea of the hybrid gate-driver scheme is to reduce the dominant switching loss with the CSD. A 12 V input, 1.0–1.5 V output, and 1 MHz synchronous buck converter was built to verify the advantages of the proposed CSD. At 1.3 V output, the proposed CSD improves the efficiency from 80.7% using a conventional driver to 85.7% (an improvement of 5%) at 20 A, and at 30 A, from 77.9% to 84.4% (an improvement of 6.5%).

In addition, the proposed CSD can also achieve gate energy recovery. Two paralleled SR MOSFETs (IRF6691$\times$2) were used to verify gate energy recovery with different switching frequencies and gate-driver voltages. At $V_D = 7$ V and the switching frequency of 2 MHz, the gate loss reduction with the CSD is as much as 2.24 W, a reduction of 63% with the conventional driver. The wide operation range of duty cycle and switching frequency were also verified by the experiment results.

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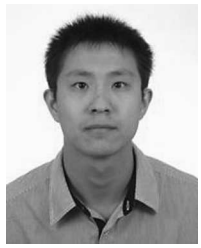

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